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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,678	07/08/2005	Hisao Kunitani	2005 _1063A	8361

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/541,678	KUNITANI ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07-08-05;08-24-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: the disclosure " the phase control circuit shifts the phase of the clock of the present reference signal at a clock rate interval equivalent to a (I-N)/N clock so as to bring the phase of the present reference signal close to the phase of the previous reference signal" on page 6, 3rd paragraph is misleading. Figure 1 of the present application shows that the phase control circuit (12) shifts the output of the comparison circuit (11); and the output of the comparison circuit (11) is not the present reference signal (9). The output of circuit (11) is the result of the comparison of the previous reference signal and the present reference signal. Therefore, the phase control circuit does not shift the phase of the clock of the present reference signal at a clock rate interval equivalent to a (1-N)/N clock so as to bring the phase of the present reference signal close to the phase of the previous reference signal". The Applicant is requested to explain the meaning of "(1-N)/N clock". The disclosure "According to Claim 9 of the present invention, in the semiconductor device defined in any of Claims 1 to 7, the phase control circuit counts the number of clocks in units of 1/M-lines (M: integer not less than 2), and performs the phase control on the basis of the count value. Therefore, the phase of the clock of the present reference signal can be controlled in units of 1/M-lines" is confusing. The Applicant is requested to explain what the disclosure "counts the number of clocks in units of 1/M-lines (M: integer not less than 2)" and "the phase of the clock of the present reference signal can be controlled in units of 1/M-lines" are meant by.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and or clarification is required.

Regarding claim 1, the recitation " using N stages of delay cells each by 1/N clock" on line 2 is indefinite because it is not clear what "1/N clock" is meant by. As understood by one of ordinary skill in the art, a delay circuit delays a signal by a certain amount period of time, not by an amount of clock. Clear explanation is required. The recitation "...and the previous reference signal that is one line previous to the present reference signal" on lines 8-9 is indefinite because it is not clear what "one line previous to the present reference signal" is meant by. The Applicant is requested to shows the drawing that explains this recitation. The recitation "a phase control circuit for shifting the phase state of the present reference signal to make it coincide with the phase state of the previous reference signal, when the comparison circuit detects that the phase states of the present reference signal and the previous reference signal do not coincide with each other" on lines 12-13 is indefinite because it is confusing. Figure 1 of the present application shows that the phase control circuit (12) shifts the output of the comparison circuit (11); and the output of the comparison circuit (11) is not the present reference signal (9). The output of circuit (11) is the result of the comparison of the previous reference signal and the present reference signal. Circuit (12) cannot make the present reference signal coincides with the phase state of the previous reference signal as recited. The recitation "the selector" on line 16 lacks antecedent basis.

Claim 2 and 3 are indefinite because the phase control circuit (12) has no clock input, thus, it cannot count up/down the number of clock stepwisely as recited.

Regarding claim 4, the recitation "said phase control circuit shifts the phase of the clock of the present reference signal at a clock rate interval equivalent to a (1+N)/N" is indefinite because it is misdescriptive. This recitation is a phrase on page 6, 3rd paragraph of the specification. Figure 1 of the present application shows that the phase control circuit (12) is connected to the output of the comparison circuit (11). The output of the comparison circuit is the result of the comparison of the present reference signal and the previous reference signal. Therefore, the said phase control circuit does not shift the phase of the clock of the present reference signal at a clock rate interval equivalent to a (1+N)/N". The Applicant is requested to explain the meaning of " (1+N)/N". Clear explanation is required. The same rationale is applied to claims 5-7. The phase control does not shift the phase of the clock of the "present reference signal " as recited. The Applicant is requested to show the drawings

that justify the definiteness of claims 4-7. The Applicant is requested to explain the meaning of " (1-N)/N" in claim 5.

Regarding claim 8, the recitation "said phase control circuit counts the number of clocks clock by clock" is indefinite because it is not clear what "...counts the number of clocks clock by clock" is meant by.

Regarding claim 9, the recitation " wherein said phase control circuit counts the number of clocks in units of 1/M-lines (M: integer not less than 2), and performs the phase control on the basis of the count value" is indefinite because it is confusing. It is not clear what the recitation "...in units of 1/M-lines" is meant by.

Regarding claim 10, the recitation "wherein said phase control circuit counts the number of clocks line by line, and performs the phase control on the basis of the count value" is indefinite because it is not clear what "counts the number of clocks line by line" is meant by.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Jung (US 6,342,796).

Regarding claim 1, 2 and 3, figure 2 of Jung show a semiconductor device for shifting an input clock comprising: a reference signal phase detection circuit (230, 240), a comparison circuit (270), a phase control circuit (280) and a phase selector control circuit (290, 300).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen
11-01-06

TUAN T. LAM
PRIMARY EXAMINER